Amendments To The Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising:

providing a semiconductor wafer having a plurality of integrated circuit dice formed therein, the integrated circuit dice including a plurality of electrically conductive contact pads and solder-wettable electrically conductive trim pads exposed on an active surface of the wafer, wherein the trim pads are not covered by a passivation layer;

forming contact bumps on a plurality of the contact pads, wherein the solder-wettable electrically conductive trim pads are exposed on the active surface of the wafer during the forming of the contact bumps;

probing the wafer after the contact bumps have been formed, wherein the wafer probing includes,

a trimming operation that includes directly probing solder-wettable portions of the plurality of exposed solder-wettable electrically conductive trim pads and trimming selected circuits associated with selected trims pads, and

a testing operation that involves probing at least some of the plurality of contact bumps to test selected functionalities of the integrated circuits; and

applying an electrically insulating undercoating to the active surface of the wafer that directly contacts and covers the solder-wettable trim pads while leaving at least portions of the contact bumps exposed, the undercoating being applied after the wafer probing, whereby the wafer may be trimmed and tested at substantially the same stage of wafer processing.

2. (Original) A method as recited in claim 1 wherein the probing for the trimming and testing operations is performed sequentially.

3. (Original) A method as recited in claim 1 wherein the probing for the trimming and testing operations are performed substantially simultaneously.

4. (Original) A method as recited in claim 1 wherein the undercoating is formed from a material selected from the group consisting of: epoxies, polyimides, and silicone-polyimide copolymers.

5. (Original) A method as recited in claim 1 wherein the undercoating has a final thickness in the range of approximately 0.2 and 4 mils.

6. (Original) A method as recited in claim 1 wherein the undercoating is formed from an underfill material that is suitable for filling a region between a die and a substrate that the die is mounted to after the wafer has been diced and the die mounted to the substrate.

7. (Original) A method as recited in claim 1 wherein the undercoating is formed from a B-stageable material.

8. (Original) A method as recited in claim 1 wherein the undercoating is formed from a curable material, the method further comprising curing the undercoating to permanently affix the undercoating to the surface of the wafer.

9. (Original) A method as recited in claim 1 wherein the undercoating is applied by one of a spin-on coating process, a molding process, a screen printing process and a stencil printing process.

10-15. (Cancelled)

16. (Currently Amended) A method as recited in claim 1 wherein the contact pads ~~have~~ each include a metallization stack ~~stacks formed thereon~~.

17. (Currently Amended) A method as recited in claim 16 wherein the trim pads ~~have~~ each include a metallization stack ~~stacks formed thereon~~.

18. (Previously Presented) A method as recited in claim 1 further comprising dicing the wafer after the undercoating has been applied to provide a multiplicity of singulated dice each having an undercoat thereon.

19. (New) A method comprising:

providing a semiconductor wafer having a plurality of integrated circuit dice formed therein, the integrated circuit dice including a plurality of electrically conductive contact pads and solder-wettable electrically conductive trim pads exposed on an active surface of the wafer, wherein the trim pads are not covered by a passivation layer;

forming contact bumps on a plurality of the contact pads, wherein the solder-wettable electrically conductive trim pads are exposed on the active surface of the wafer during the forming of the contact bumps;

probing the wafer after the contact bumps have been formed, wherein the wafer probing includes,

a trimming operation that includes directly probing solder-wettable portions of the plurality of exposed solder-wettable electrically conductive trim pads and trimming selected circuits associated with selected trims pads, and

a testing operation that involves probing at least some of the plurality of contact bumps to test selected functionalities of the integrated circuits; and

applying an electrically insulating undercoating to the active surface of the wafer that directly contacts and covers the solder-wettable trim pads while leaving at least portions of the contact bumps exposed, the undercoating being formed from a polymer based adhesive material selected from the group consisting of: epoxies, polyimides, silicone-polyimide copolymers, and BCB and wherein,

the undercoating has a final thickness in the range of approximately 0.2 and 4 mils.

the undercoating is applied after the wafer probing, whereby the wafer may be trimmed and tested at substantially the same stage of wafer processing; and

dicing the wafer after the undercoating has been applied to provide a multiplicity of singulated dice each having an undercoat thereon.